PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	32

Application Number	09/800,841
Filing Date	03/06/2001
First Named Inventor	Rohit Kapur
Art Unit	2133
Examiner Name	James C. Kerveros
Attorney Docket Number	SYN-0174#2

ENCLOSURES *(check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Terminal Disclaimer
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Statement Under 37 CFR 3.73(b)
- ☐ CD, Number of CD(s) _____
- ☐ Request for Refund

Remarks

- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to TC *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) *(please identify below):*

Return Receipt Postcard

SIGNATURE OF APPLICANT, ATTORNEY OR AGENT

Firm Name	BEVER, HOFFMAN & HARMS, LLP	Customer Number	35273
Signature			
Printed Name	Jeanette S. Harms		
Date	April 26, 2005	Reg. No.	35,537

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature	Rebecca A. Baumann		
Typed or printed name	Rebecca A. Baumann	Date	April 26, 2005

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMV 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818)

FEE TRANSMITTAL For FY 2005

MAY 02 2005

☒ Applicant claims small entity status. See 37 C.F.R. § 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	09/800,841
Filing Date	03/06/2001
First Named Inventor	Rohit Kapur
Examiner Name	James C. Kerveros
Art Unit	2133
Attorney Docket No	SYN-0174#2

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify):_____

☒ Deposit Account Deposit Account Number: **50-0574** Deposit Account Name: **Bever, Hoffman & Harms, LLP**

For the above-identified deposit account, the Director is hereby authorized to; (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	**Fees Paid ($)**
Utility	300	150	500	250	200	100	$
Design	200	100	100	50	130	65	$
Plant	200	100	300	150	160	80	$
Reissue	300	150	500	250	600	300	$
Provisional	200	100	0	0	0	100	$

2. EXCESS CLAIM FEES

Fee Description	Fee($)	Small Entity Fee($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee($)	**Fee Paid ($)**	Multiple Dependent Claims		
	- 20 or HP =	x	=		Fee($)	Fee($)

HP = highest number of total claims paid for, if great than 20

Indep. Claims	Extra Claims	Fee($)	**Fee Paid ($)**
	- 3 or HP =	x	=

HP = highest number of total claims paid for, if great than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 USC 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee($)	Fee Paid ($)
- 100 =	5- = (round up to a whole number) x		=	

4. OTHER FEE(S)

	Fee Paid ($)
Non-English Specification - $130 fee (no small entity discount)	
Other: **APPEAL BRIEF**	**$500.00**

SUBMITTED BY

Signature:	Registration No. 35,537	Telephone: (408) 451-5907
Name (Print/Type) Jeanette S. Harms		Date: April 26, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rohit Kapur and Thomas Williams

Assignee: Synopsys, Inc.

Title: SYSTEM AND METHOD FOR AUTOMATICALLY RETARGETING TEST VECTORS BETWEEN DIFFERENT TESTER TYPES

Serial No.: 09/800,841 File Date: March 6, 2001

Examiner: James C. Kerveros Art Unit: 2133

Docket No.: SYN-0174#2

April 26, 2005

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

This Appeal Brief, filed in triplicate, is in support of the Notice of Appeal dated April 18, 2005.

/

/

/

/

/

/

/

/

/

/

INDEX

I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Synopsys, Inc., pursuant to the Assignment recorded in the U.S. Patent and Trademark Office on January 4, 2002 on Reel 012431, Frame 0339.

II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no other appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-29 are pending. Claims 1-29 stand rejected.

In the present paper, rejected Claims 1-29 are appealed.

Pending Claims 1-29 are listed in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Claims 1, 3, 8, 10, 17, and 25 were amended after the First Office Action. These amendments are now entered.

V. SUMMARY OF THE CLAIMED INVENTION

As taught by Applicants on page 3, lines 5-20 of the Specification:

> testing systems, or "testers" are used to apply test vectors to a device under test, capture the test results and shift them out for examination and comparison. However, as with any resource, test facilities have testers of different capabilities and configurations. The testers differ in their clocking characteristics, their power supply capabilities, their memory resources used behind each pin, and most importantly, they [differ] in the number of pins that can supply and receive scan data and functional inputs/outputs, etc. Typically, the more pins available on a tester, the more expensive the tester equipment. For example, today testers cost approximately $5,000.00 per pin supported. The more pins the tester can drive, the more scan chains a design can implement. The more scan chains available, the shorter the scan chains can be, thereby reducing the time it takes to load them up. Conversely, a tester with few pins only supports a design having fewer but longer scan chains. Therefore, testers with high pin count can drive many scan chains and the more scan chains available, the shorter they can be, the faster they load and the more economical the test.

As further taught by Applicants on page 4, line 23 to page 5, line 11 of the Specification:

> Although testers vary in pin capacity, nevertheless, the test data generated by ATPG processes is typically generated in an environment that is oblivious to the tester capabilities. For example, in many cases, test patterns tend to be routinely developed for high performance testers without knowing the capabilities of the test facility. This is done because most test engineers are geared to reduce test application time. However, to limit costs, a test facility typically acquires some low cost

> testers and some high cost testers, which differ in the number of full functional pins they have. If a test facility (e.g., having a mix of both high and low capacity testers) receives test vectors developed for high performance testers, the result will be that many of their low cost testers are left idle because of test vector incompatibility. Having any of these testers idle is waste of resources and money. It would be advantageous, then, to provide a system tat can make full use of the various different types of testers that facility has but is based on a single set of developed test vectors.

In accordance with one aspect of the invention, on-chip circuitry can automatically reconfigure the number and the size of the scan chains within an integrated circuit depending on the performance mode selected. Specification, page 7, lines 10-12. Notably, the present invention can be applied to numerous configurations of the design, with different pin counts and requirements from the tester. Specification, page 18, lines 5-6. For example, Figures 4A and 4B (shown below) illustrate exemplary devices under test.

In Figure 4A, two modes of operation are supported, high performance and low performance. Specification, page 18, lines 1-15. In a high performance mode (selector 270a is low), scan chains 310a and 310b receive inputs from scan inputs 320a and 320b, respectively, and scan data out using scan outputs 340a and 340b, respectively. In contrast, in a low performance mode (selector 270a is high), scan input 320a and scan output 340b are ignored. Specification, page 19, lines 10-12. Thus, two scan chains independently function in the high performance mode whereas only one scan chain (scan chains 310a and 310b connected in series) functions in the low performance mode. This configuration is scalable, wherein for a typical implementation, the scan and mux circuitry would be replicated many times over

with all muxes having their select lines coupled together to provide the performance adjustments. Specification, page 20, lines 4-9.

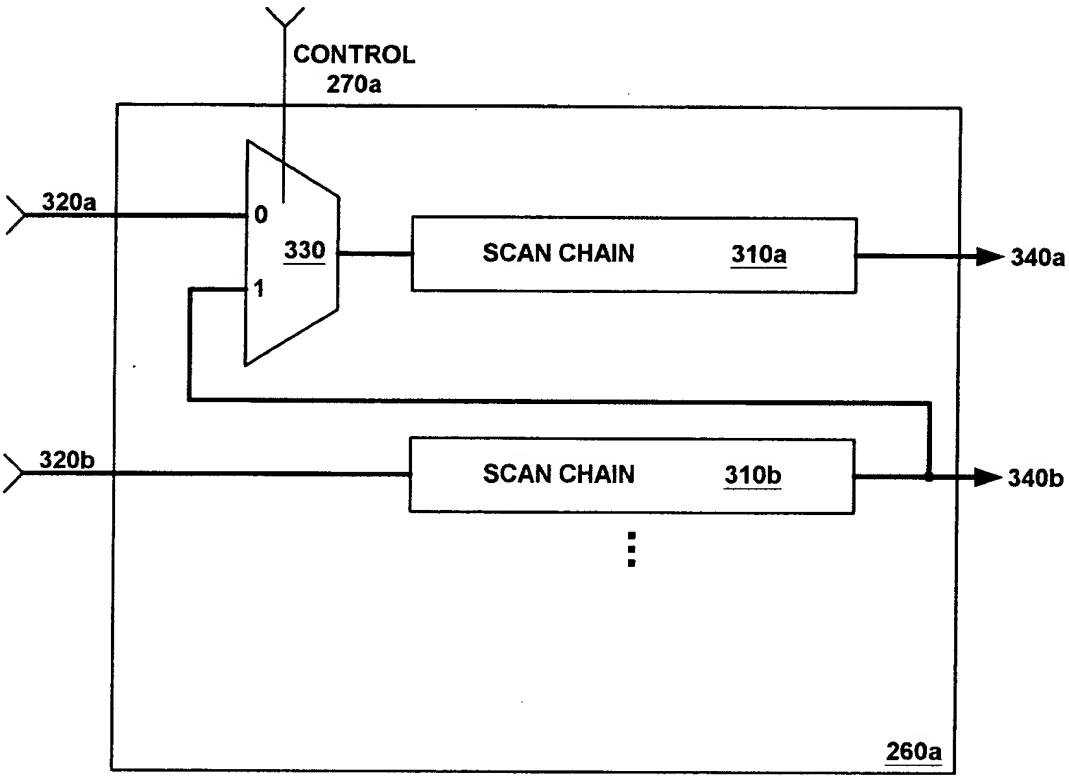


FIGURE 4A

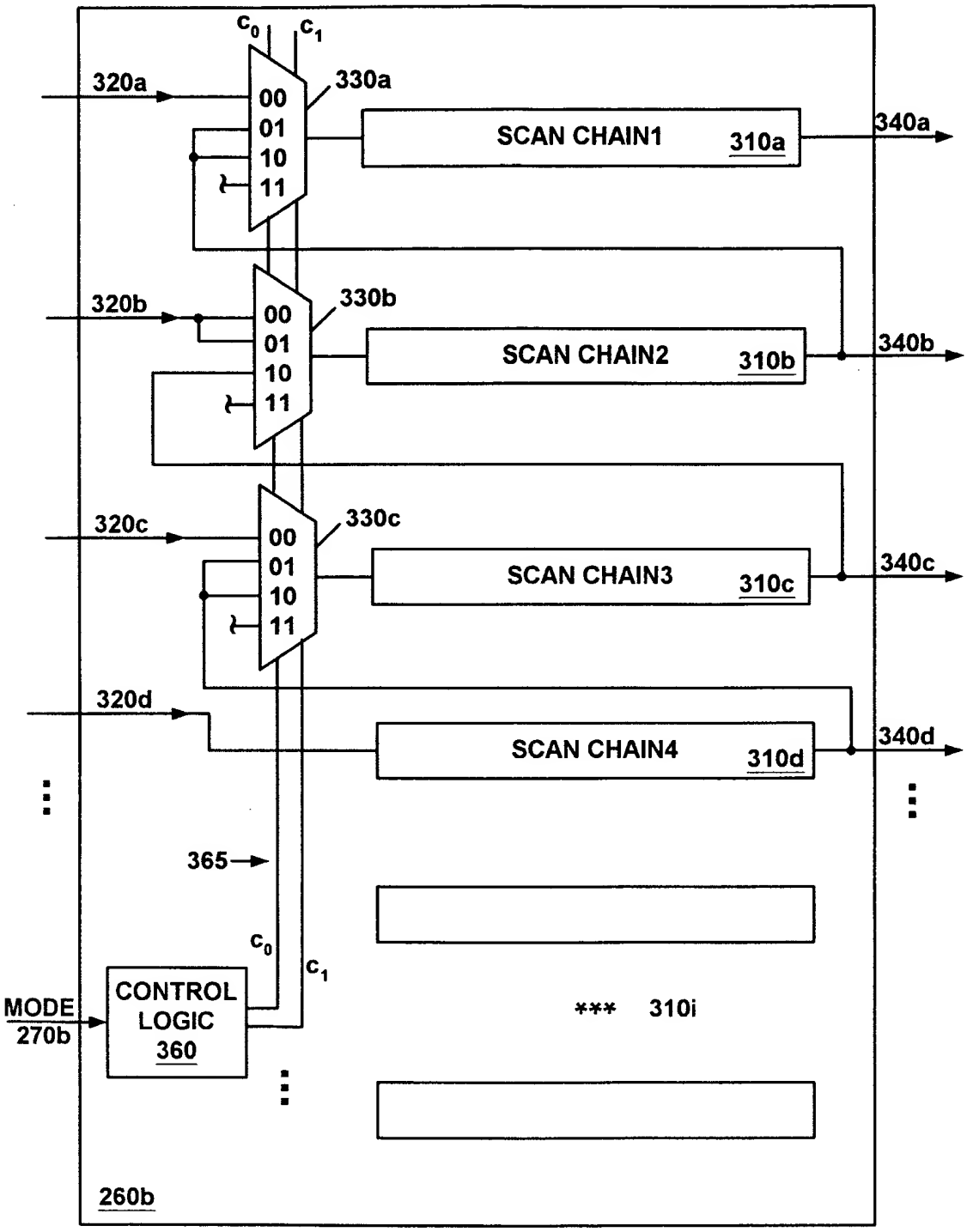

C_0
C_1
320a
330a
00
01
10
11
SCAN CHAIN1
310a
340a
320b
330b
SCAN CHAIN2
310b
340b
320c
330c
SCAN CHAIN3
310c
340c
320d
SCAN CHAIN4
310d
340d
365
MODE
270b
CONTROL
LOGIC
360
*** 310i
260b

FIGURE 4B

In Figure 4B, three modes of operation are supported, high performance, medium performance, and low performance. Specification, page 20, lines 11-21. In a high performance mode, there are four separate scan chains (310a, 310b, 310c, and 310d). In a medium performance mode, there are two separate scan chains (chain 310a + 310b, chain 310c + 310d). In a low performance, there is a single scan chain (chain 310a + 310b + 310c + 310d). This configuration is also scalable, wherein for a typical implementation, the configuration of Figure 4B can be replicated many times over with common muxes having the same control lines coupled thereto. Specification, page 20, lines 19-21.

Referring to Claim 1, the scan chains can include scan chains 310 of Figures 4A and 4B, and the reconfiguration logic can include multiplexers 330 and control logic 360 (also shown in Figures 4A and 4B). The test vectors and testers 220 having first and second pin capacities are shown generally in Figure 3. See also, e.g. Specification, page 15, lines 14-24; page 16, lines 4-25; page 18, lines 13-17; and page 20, lines 11-21.

Referring to Claims 2, 9, and 24, the second pin capacity being less than a first pin capacity is shown in Figure 3 (e.g. 64 or 1000). See also, e.g. Specification, page 15, lines 20-24.

Referring to Claims 3, 10, and 25, the second pin capacity being a low pin count and the first pin capacity being a high pin count is generally shown in Figure 3 (e.g. 64 or 1000). See also, e.g. Specification, page 15, lines 20-24.

Referring to Claims 6, 13, 20, and 28, the respective multiplexers for each memory cell of the functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said mode signal can

include multiplexers 450 for each memory cell 440 as shown in Figure 5. See also, e.g. Specification, page 23, lines 8-11, and 18-24.

Referring to Claims 7, 14, and 21, the protocol unit coupled to the mode signal and comprising a first test sequence used for the tester of the first pin capacity and a second test sequence used for the tester of the second pin capacity can include the protocol unit 210 coupled to said mode signal 270 as shown in Figure 3. See also, e.g. page 16, lines 17-25.

Referring to Claims 8 and 15, the storage medium can include high performance test vectors storage 230 (Figure 3), the selector can include user adjustable performance mode selector 240 (Figure 3), the device under test can include IC device 260 (Figure 3), the scan chains can include scan chains 310 (Figures 4A and 4B), and the reconfiguration logic can include multiplexers 330 (Figures 4A and 4B) and control logic 360 (Figure 4B). See also, e.g. page 15, line 14 to page 22, line 25.

Referring to Claim 16, the reconfiguration logic that can decrease the number of pins required to test the device under test for a test mode that is used for the tester having the low pin capacity can include multiplexers 330 (Figures 4A and 4B) and control logic 360 (Figure 4B). See also, e.g. page 18, lines 13-15; page 19, lines 8-13 and 18-24; and page 20, lines 1-2.

Referring to Claim 17, the low pin capacity being more than 64 pins and the high pin capacity being more than 1000 pins can be shown in Figure 3 (i.e. 64+ and 1000+). See also, e.g. Specification, page 15, lines 20-24.

Referring to Claim 22, the steps of storing, selecting, and altering can be performed by the components shown in Figure 3. See also, e.g. page 15, line 14 to page 17, line 19.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented to the Board of Appeals for decision:

(A) Whether Claims 1-29 comply with the written description requirement of 35 U.S.C. 112, first paragraph.

(B) Whether Claims 1, 4-8, 11-15, 18-23, and 26-29 are patentable under 35 U.S.C. 102(e) over U.S. Patent 5,983,380 (Motika).

(C) Whether Claims 2, 3, 9, 10, 16, 17, 24, and 25 are patentable under 35 U.S.C. 103(a) over Motika in view of U.S. Patent 6,311,300 (Omura).

VII. ARGUMENTS

A. Claims 1-29 comply with the written description requirement of 35 U.S.C. 112, first paragraph

The Office Action states that the claims contain subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor, at the time the application was filed, had possession of the claimed invention. The Office Action further states that the specification fails to describe the new limitation "wherein the number of said scan chains can be greater than one and less than a maximum number". The Office Action yet further states that the specification "fails to clearly specify the number of the scan chains, so as to enable a person skilled in the art to

calculate a range for the scan chains 'of greater than one and less than a maximum number'".

Applicants respectfully disagree. This remark highlights an important advantage of Applicants' invention. That is, the number and length of the scan chains in a design under test can be advantageously configured for use with different testers. Because the number and length of the scan chains can be configured, an exact number of scan chains should not be required in the broadest claims. Figures 4A and 4B (shown above) illustrate exemplary devices under test, which could have a different number of scan chains depending on their configuration. As indicated in the Specification, these device configurations are scalable. Specification, page 20, lines 4-9 and 19-21. Thus, by providing the appropriate configuration logic (e.g. scan and multiplexer circuitry), a design under test can be configured to provide N scan chains, wherein N can be greater than one and less than a maximum number of scan chains. For clarity, an example is provided of how one skilled in the art would compute N for a design. Specifically, for a 4 input multiplexer having 4 inputs and 2 select wires to select among the four inputs (i.e. a total of 6 signals), to exhaustively test every possible input, a user would need $2^{(4+2)} = 2^6 = 128$ possible tests.

Applicants respectfully submit that the maximum number of scan chains is not an arbitrary number as characterized in the Office Action. Specifically, the maximum number of scan chains can be based on the number of pins available as well as the design being implemented, which is known to those skilled in the art. Thus, the maximum number of scan chains may vary based on a chip/design combination, but is not arbitrary in any sense. Therefore, Applicants respectfully submit that those skilled in

the art would understand the term "maximum number of scan chains".

Based on the above remarks, Applicants submit that Claims 1-29 comply with the written description requirement of 35 U.S.C. 112, first paragraph.

B. Claims 1, 4-8, 11-15, 18-23, and 26-29 are patentable under 35 U.S.C. 102(e) over U.S. Patent 5,983,380 (Motika)

1. Motika Overview

> [Motika teaches] an integrated circuit comprising logic circuits and self-test circuits for testing the logic circuits. The self-test circuits include a pseudo random pattern generator for generating at least one pseudo random pattern and a weighing circuit for weighing the pseudo random pattern. The weighing circuit includes an input for receiving a weighing instruction for selectively weighing the pseudo random pattern so that the weighing circuit and the pseudo random pattern generator generate at least one weighted pseudo random pattern for testing the logic circuits.

Col. 3, lines 17-27.

Fig. 3 of Motika (shown below) illustrates an externally selectable WRPBIST (weighted random pattern built-in self test) structure. Col. 4, lines 11-13. As taught by Motika in col. 5, lines 43-55:

> Linear feedback shift register (LFSR) 12 is utilized to supply the flat pseudo random patterns to WRP generation sub functions 118, 120, 122, 124 and 126. The output of each WRP sub function 118, 120, 122, 124 and 126 feed BS chain 128, STCM chain 130 and SRL chains 132, 134, 136. A "global weight set select" register 138 provides the common selection of the WFP. SRI data or test vector 140 select the desired true or complement probabilities for each chain 128, 130, 132, 134, 136. A "mode select" signal from a

> mode select register 142 allows for normal LSSD or WRPLBIST test mode. The rest of the STUMPS structure, including the signature analysis (MISR) 16 remains unchanged from that shown in FIG. 1.

Notably, in the LSSD mode, the multiplexers are set to essentially form one serpentine scan chain having a length of all the scan chains, i.e. forming a single scan chain. In contrast, in the WRPLBIST test mode, the multiplexers are set to provide weighted random patterns (WRPs) to each of the scan chains. Thus, the number of scan chains in this mode is equal to the maximum number of scan chains. Therefore, in summary, Motika teaches only two scan chain lengths: one or the maximum number.

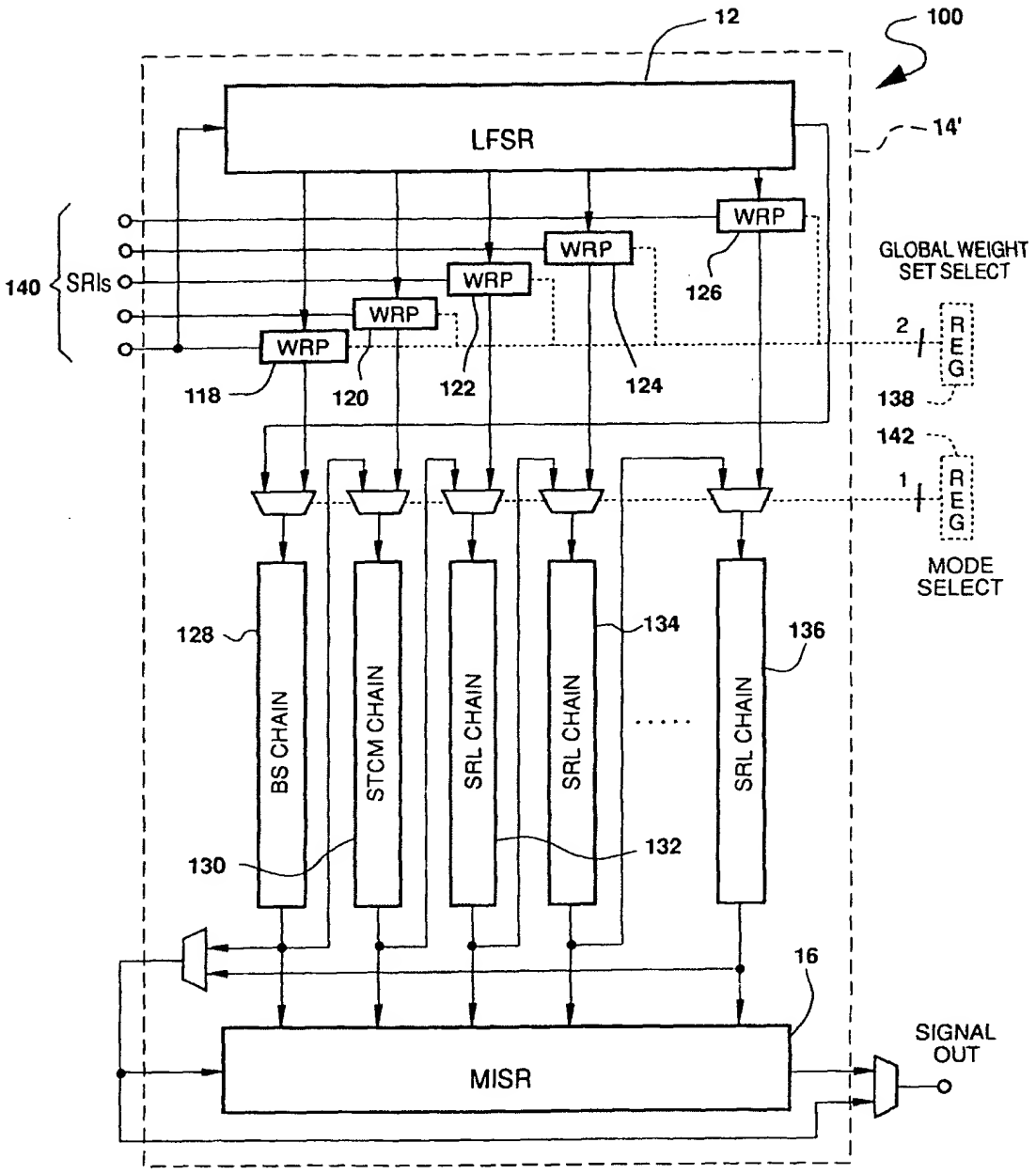


FIG - 2

2. Applicants' limitations recited in Claims 1, 4-8, 11-15, 18-23, and 26-29 are not taught by Motika.

Claim 1 recites in part:

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on a mode signal, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said second tester having said second pin capacity, said mode signal selecting between said first tester and said second tester.

Claim 8 recites in part:

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on said user selector, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said tester having said second pin capacity.

Claim 15 recites in part:

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on said test mode, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said tester having said low pin capacity.

Claim 22 recites in part:

c) in response to said step b), altering the number of pins required to test said device under test by reconfiguring the individual length and number of scan chains internal to said device based on said test mode, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, wherein

said altering provides compatibility between said test vectors and said tester having said second pin capacity.

As taught by Applicants, configurations of the design may include different pin counts and requirements from the tester. Specification, page 18, lines 4-6. In one configuration, a high pin count is used including individual functional inputs and many balanced scan chains for low test application time. Specification, page 18, lines 7-9. In another configuration, a very low pin count can be achieved at the trade-off of higher test application times caused by longer scan chains. A user-adjustable test mode selector allows reconfiguration of the on-chip circuitry, thereby ensuring compatibility with testers of different pin capacities. Specification, page 16, lines 4-11. Notably, Applicants' invention can make full use of the various different types of testers that a test facility has but uses a single set of developed test vectors. Specification, page 6, lines 2-4.

Motika fails to disclose or suggest this limitation and its advantages. Specifically, Motika teaches that a mode select signal allows for normal LSSD or WRPLBIST test modes. Col. 5, lines 51-53. Thus, referring to Fig. 2 of Motika, in the LSSD mode, the multiplexers are set to essentially form one serpentine scan chain having a length of all the scan chains (i.e. forming a single scan chain). In contrast, in the WRPLBIST test mode, the multiplexers are set to provide weighted random patterns (WRPs) to each of the scan chains. Thus, the number of scan chains in this mode is equal to the maximum number of scan chains.

In general, Motika teaches test methodologies that allow for three distinct test modes. Col. 2, lines 48-49. In a first mode based on deterministic LSSD and test techniques described

in U.S. Patent 3,783,254, the test supplies the patterns to be loaded in each SRL (shift register latch) chain and then pulses the appropriate system clocks. Col. 2, lines 52-55. In a second mode based on WRP (weighted random pattern) methodology, an LFSR (linear feedback shift register) algorithmically generates a set of pseudo random test patterns at the tester. Col. 2, lines 58-63. These patterns are then weighted to optimize them for a specific logic design. Col. 2, lines 63-64. In a third mode, some of these techniques can be extended to BIST (built in self test) and incorporates the LFSR and a MISR (multiple input signature register) in the DUT. Col. 3, lines 3-5. Motika attempts to balance these three test modes. Col. 3, lines 10-13.

Fundamentally speaking, Applicants' recited device/method/system ties patterns to configurations in such a way that the same test patterns can be executed through different interfaces. In contrast, Motika's teaching applies different patterns and test methodologies implemented on the same design, which has nothing to do with efficiency of applying the same tests for efficient utilization of ATE resources. Therefore, in particular, Motika fails to disclose or suggest compatibility between said test vectors as well as the reconfiguration logic for altering the number of pins required to test the DUT by reconfiguring the individual length and number of said scan chains based on the test mode, wherein the number of scan chains can be greater than one and less than a maximum number of scan chains.

Because Motika fails to teach various recited limitations, Applicants submit that Claims 1, 8, 15, and 22 are patentable over Motika.

Claims 4-7 depend from Claim 1, Claims 11-14 depend from Claim 8, Claims 18-21 depend from Claim 15, and Claim 23 and 26-

29 depend from Claim 22. Therefore, Claims 4-7, 11-14, 18-21, 23, and 26-29 are patentable for at least the reasons presented for Claims 1, 8, 15, and 22.

Moreover, Claims 6, 13, 20, and 28 recite, wherein said reconfiguration logic also comprises "a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin" based on the mode signal (Claim 6), user selector (Claim 13), the test mode (Claim 20), or the test mode selected (Claim 28). The MUX 146 of Motika, cited in the Office Action, as teaching the recited multiplexer, is not for each memory cell of LFSR 12. Therefore, Motika also fails to teach these recited limitations.

Moreover, Claims 7, 14, and 21 recite, "a protocol unit" coupled to the mode signal (Claim 7) or the user selector (Claims 14 and 21) and "comprising a first test sequence used for said tester of said first pin capacity and a second test sequence used for said tester of said second pin capacity". Motika teaches that the WRP patterns are generated by the tester externally to the DUT and loaded via the shift register inputs (SRIs) into the chip's shift register latches (SRLs). Col. 4, lines 63-66. Applicants note that the global weight set select register 138 (cited in the Office Action as teaching this protocol unit) fails to teach the first and second test sequences. Therefore, Motika also fails to teach these recited limitations.

C. Claims 2, 3, 9, 10, 16, 17, 24, and 25 are patentable under 35 U.S.C. 103(a) over Motika in view of U.S. Patent 6,311,300 (Omura).

1. Motika: Overview (see Section B)

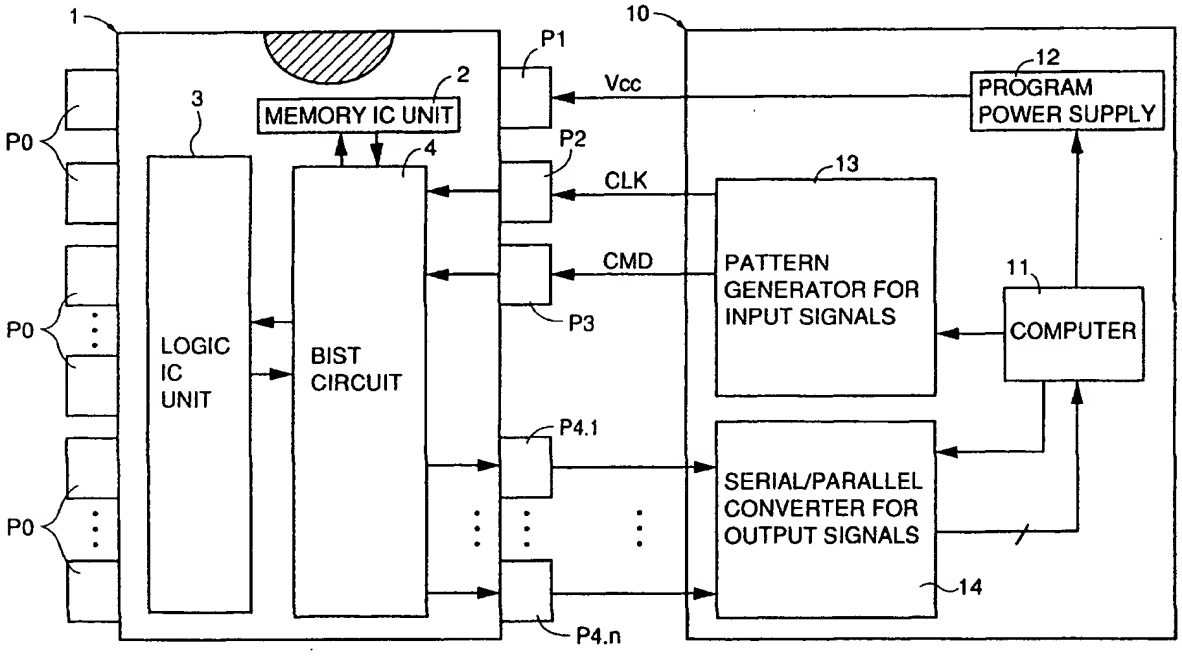
2. Omura: Overview

As Omura teaches in the Abstract:

> A program power supply of a tester applies a power supply voltage to an IC to be tested. A pattern generator applies a clock signal and a command signal to a BIST circuit of IC. BIST circuit tests memory IC unit and logic IC unit and serially outputs data indicative of test result to a converter of tester. Converter converts the applied serial data to parallel data and applies to computer. As compared with the prior art in which address signal and control signal are applied to IC to be tested, the number of pins necessary for the test can be reduced. Therefore, cost of the test is reduced and efficiency of the test is improved.

Fig. 1 (shown below) illustrates an exemplary tester 10 and integrated circuit (IC) 1 in accordance with the teaching of Omura. Col. 3, lines 38-40.

FIG. 1



3. Applicants' limitations recited in Claims 2, 3, 9, 10, 16, 17, 24, and 25 are not taught by Motika and Omura combined.

Claims 2-3 depend from Claim 1, Claims 9-10 depend from Claim 8, Claims 16-17 depend from Claim 15, and Claim 25 depends from Claim 22. Therefore, Claims 2-3, 9-10, 16-17, and 24-25 are patentable for at least the reasons presented for Claims 1, 8, 15, and 22.

Omura fails to remedy the deficiencies of Motika with respect to Claims 1, 8, 15, and 22. Specifically, Omura teaches providing a BIST (built in self test) in a semiconductor device having a memory circuit and in a semiconductor test apparatus including a power supply for applying a power supply voltage to the semiconductor device, an instructing circuit for instructing execution of a test and output of data indicative of the test result to the self test circuit, and a receiving circuit for receiving data output from the self test circuit. Col. 2, lines 30-39. According to Omura, this configuration reduces the number of terminals for signal output and the number of pattern generators and increases the number of semiconductor devices that can be tested on one time per one semiconductor testing apparatus. Col. 2, lines 39-46.

Therefore, Omura also fails to disclose or suggest compatibility between the recited test vectors as well as the reconfiguration logic for altering the number of pins required to test the DUT by reconfiguring the individual length and number of said scan chains based on the test mode, wherein the number of scan chains can be greater than one and less than a maximum number of scan chains.

Because Motika and Omura in combination fail to disclose or suggest the recited limitations in Claims 1, 8, 15, and 22,

Applicants respectfully submit that Claims 2-3, 9-10, 16-17, and 24-25, which depend from Claims 1, 8, 15, and 22, are patentable over the cited references.

Moreover, Claims 2, 9, and 24 recite:

> wherein said second pin capacity is less than said first pin capacity.

Claims 3, 10, and 25 recite:

> wherein said second pin capacity is a low pin count and said first pin capacity is a high pin count.

Claim 16 recites:

> wherein reconfiguration logic decreases the number of pins required to test said device under test for a test mode that is used for said tester having said low pin capacity.

Claim 17 recites:

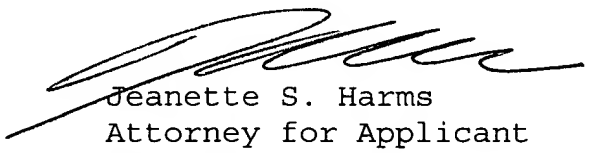
> wherein said low pin capacity is more than 64 pins and said high pin capacity is more than 1000 pins.

The Office Action apparently cites pin electronics 61 of Omura as teaching these limitations. Applicants traverse this characterization. Omura teaches that pin electronics 61 includes a driver, a comparator, and a group of relays connecting these to IC 70 to be tested, and is coupled to IC 70 to be tested through a contact terminal 71. Col. 1, lines 62-65. This passage teaches nothing regarding the recited limitations. Because neither Motika nor Omura disclose or suggest these limitations, Claims 2-3, 9-10, 16-17, and 24-25 are further patentable over the cited references.

D. CONCLUSION

For the foregoing reasons, it is submitted that the Examiner's rejections of Claims 1-29 are erroneous, and reversal of these rejections is respectfully requested.

Respectfully submitted,



Customer No.: 35273

Jeanette S. Harms
Attorney for Applicant
Reg. No. 35,537

Telephone: 408-451-5907
Facsimile: 408-451-5908

I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 26, 2005.

4/26/2005 Rebecca A. Baumann
Date Signature: Rebecca A. Baumann

VIII. CLAIMS APPENDIX

1. (Previously Presented) An integrated circuit device for communicating with a first tester of a first pin capacity to receive test vectors developed for a second tester of a second pin capacity, said device comprising:

scan chains; and

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on a mode signal, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said second tester having said second pin capacity, said mode signal selecting between said first tester and said second tester.

2. (Original) A device as described in Claim 1 wherein said second pin capacity is less than said first pin capacity.

3. (Previously Presented) A device as described in Claim 2 wherein said second pin capacity is a low pin count and said first pin capacity is a high pin count.

4. (Original) A device as described in Claim 1 wherein said reconfiguration logic comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

5. (Original) A device as described in Claim 1 wherein said reconfiguration logic comprises:

a functional input shift register for receiving functional

inputs and used for a mode corresponding to said tester of said second pin capacity; and

a functional output shift register for providing functional output values and used for said mode corresponding to said second pin capacity.

6. (Previously Presented) A device as described in Claim 5 wherein said reconfiguration logic also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said mode signal.

7. (Previously Presented) A device as described in Claim 1 further comprising a protocol unit coupled to said mode signal and comprising a first test sequence used for said tester of said first pin capacity and a second test sequence used for said tester of said second pin capacity.

8. (Previously Presented) An automated testing equipment (ATE) system for testing an integrated circuit device comprising:

a storage medium for storing a set of test vectors developed for a tester having a first pin capacity;

a user selector selecting modes between a tester having said first pin capacity and a tester having a second pin capacity; and

a device under test for coupling with one of said testers to receive said test vectors, said device under test comprising:

scan chains; and

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length

and number of said scan chains based on said user selector, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said tester having said second pin capacity.

9. (Original) A system as described in Claim 8 wherein said second pin capacity is less than said first pin capacity.

10. (Previously Presented) A system as described in Claim 9 wherein said second pin capacity is a low pin count and said first pin capacity is a high pin count.

11. (Original) A system as described in Claim 8 wherein said reconfiguration logic comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

12. (Original) A system as described in Claim 8 wherein said reconfiguration logic of said device under test comprises:

a functional input shift register for receiving functional inputs and used for a mode corresponding to said tester of said second pin capacity; and

a functional output shift register for providing functional output values and used for said mode corresponding to said second pin capacity.

13. (Previously Presented) A system as described in Claim 12 wherein said reconfiguration logic of said device under test also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a

respective memory cell and a respective functional input pin based on said user selector.

14. (Previously Presented) A system as described in Claim 8 further comprising a protocol unit coupled to said user selector and comprising a first test sequence used for said tester of said first pin capacity and a second test sequence used for said tester of said second pin capacity.

15. (Previously Presented) An automated testing equipment (ATE) system for testing an integrated circuit device, the ATE system comprising:

a storage medium for storing a set of test vectors developed for a tester having a high pin capacity;

a selector operable to select a test mode between a tester having said high pin capacity and a tester having a low pin capacity; and

a device under test for coupling with one of said testers to receive said test vectors, functional input values and said test mode and for coupling to provide test results, said device under test comprising:

scan chains; and

reconfiguration logic coupled to said scan chains and for altering the number of pins required to test said device under test by reconfiguring the individual length and number of said scan chains based on said test mode, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, said reconfiguration logic providing compatibility between said test vectors and said tester having said low pin capacity.

16. (Original) A system as described in Claim 15 wherein

reconfiguration logic decreases the number of pins required to test said device under test for a test mode that is used for said tester having said low pin capacity

17. (Previously Presented) A system as described in Claim 15 wherein said low pin capacity is more than 64 pins and said high pin capacity is more than 1000 pins.

18. (Original) A system as described in Claim 15 wherein said reconfiguration logic comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

19. (Original) A system as described in Claim 15 wherein said reconfiguration logic of said device under test comprises:

a functional input shift register for receiving functional inputs and used for a test mode corresponding with said tester of said low pin capacity; and

a functional output shift register for providing functional output values and used for said test mode corresponding with said low pin capacity.

20. (Original) A system and described in Claim 19 wherein said reconfiguration logic of said device under test also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said test mode.

21. (Previously Presented) A system as described in Claim 15 further comprising a protocol unit coupled to said user selector and comprising a first test sequence used for said

tester of said high pin capacity and a second test sequence used for said tester of said low pin capacity.

22. (Previously Presented) In an automated testing equipment (ATE) system having a device to be tested, a method for testing said device comprising the steps of:

a) storing, in a storage medium, a set of test vectors developed for a tester having a first pin capacity;

b) selecting a test mode as between a tester having said first pin capacity and a tester having a second pin capacity; and

c) in response to said step b), altering the number of pins required to test said device under test by reconfiguring the individual length and number of scan chains internal to said device based on said test mode, wherein the number of said scan chains can be greater than one and less than a maximum number of scan chains, wherein said altering provides compatibility between said test vectors and said tester having said second pin capacity.

23. (Original) A method as described in Claim 22 further comprising the step of d) applying said test vectors to said device under test using said tester having said second pin capacity.

24. (Original) A method as described in Claim 23 wherein said second pin capacity is less than said first pin capacity.

25. (Previously Presented) A method as described in Claim 24 wherein said second pin capacity is a low pin count and said first pin capacity is a high pin count.

26. (Original) A method as described in Claim 23 wherein said step c) is performed by reconfiguration logic that comprises multiplexers coupled between selected ones of said scan chains and selected scan-in pins of said device under test.

27. (Original) A method as described in Claim 26 wherein said reconfiguration logic of said device under test also comprises:

a functional input shift register for receiving functional inputs and used for a test mode corresponding with said tester of said second pin capacity; and

a functional output shift register for providing functional output values and used for said test mode corresponding with said second pin capacity.

28. (Original) A method as described in Claim 27 wherein said reconfiguration logic of said device under test also comprises a respective multiplexer for each memory cell of said functional input shift register for selecting between a respective memory cell and a respective functional input pin based on said test mode selected.

29. (Original) A method as described in Claim 23 wherein said step d) further comprises the steps of:

d1) applying a first test sequence used for said tester of said first pin capacity; and

d2) applying a second test sequence used for said tester of said second pin capacity.

IX. EVIDENCE APPENDIX

None

X. RELATED PROCEEDINGS APPENDIX

None